CLAIMS

What is claimed is:

1. A self-aligned transistor, comprising:

a first silicon portion on an isolation layer, the silicon portion having formed therein a source region and a drain region separated by a channel region, and having a first side and a second side and a top portion;

a gate oxide surrounding the channel on said first side, second side and top portion; and

a first, a second and a third silicon gate regions surrounding the first silicon portion about the first side, second side and top portion and the channel region.

2. The transistor of claim 1 wherein said first silicon portion includes an N+ source and drain region and a P-type channel region.

3. The transistor of claim 2 wherein said first portion is formed of contiguous deposited polysilicon.

4. The transistor of claim 3 wherein said second portion is formed of contiguous deposited polysilicon.

5. The transistor of claim 3 wherein said first gate, second gate, and

third gate have an N+ dopant concentration matching the source and drain regions.

6. The transistor of claim 3 wherein said first gate region has an N+ doping and the second gate region has a P+ doping.

7. The transistor of claim 1 wherein said isolation layer comprises a buried oxide region of a silicon-on-insulator substrate.

8. The transistor of claim 7 wherein said first silicon portion, first gate, and second gate are formed in a contiguous horizontal plane in said silicon-on-insulator substrate.

9. The transistor of claim 1 wherein said first silicon portion has a width in a range between 20 nanometers and 150 nanometers.

10. The transistor of claim 1 wherein a gate oxide separates said first and second silicon portions.

11. The transistor of claim 1 wherein said gate oxide has a thickness of between 1.2-1.7 nanometers.

12. The transistor of claim 1 wherein the first and second polysilicon regions are surrounded by a conformal oxide.

13. A method for manufacturing a dual gate transistor device, comprising:

(a) providing a substrate having a buried oxide region;

(b) depositing a first nitride mask layer having a pattern overlying a silicon region;

(c) forming a trench in said substrate with a depth to said buried oxide;

(d) depositing a conformal oxide in said trench;

(e) forming vias in said conformal oxide adjacent to said silicon region and removing a portion of said first nitride mask to expose a portion of said silicon region;

(f) depositing polysilicon in said vias and on said portion of said silicon region; and

(g) implanting an impurity into exposed portions of polysilicon in said trench and of said silicon-on-insulator substrate underlying said second nitride layer.

14. The method of claim 13 wherein said step (c) is performed by: depositing a nitride mask layer; forming a trench window in said nitride

mask layer; and etching said substrate to expose said buried oxide.

15. The method of claim 13 wherein said step (d) is performed by: depositing a TEOS layer to fill the trench to a level equivalent to said first nitride mask layer.

16. The method of claim 13 wherein said step (e) comprises: depositing a gate layer; and

etching the vias and the first nitride layer through an opening formed in said gate layer.

17. The method of claim 13 wherein said step (f) comprises implanting arsenic at an energy of 15-20 KeV with a zero degree tilt to provide a concentration of 2-4x1015/cm-2.

18. The method of claim 13 wherein said step (f) comprises depositing phosphorous at an energy of 7-10 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-4x1015/cm-2.

19. The method of claim 13 wherein said step (f) comprises depositing boron at an energy of 1.5-2.5 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-3x1015/cm-2.

20. The method of claim 13 further including the step, between steps (f) and (g), of:

polishing the polysilicon and substrate.

21. The method of claim 13 further including the step, between said steps (e) and (f), of:

growing a gate oxide about the silicon region in said vias.